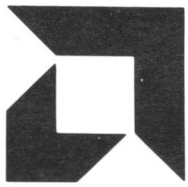
ADVANCED MICROPROCESSOR COMPONENTS

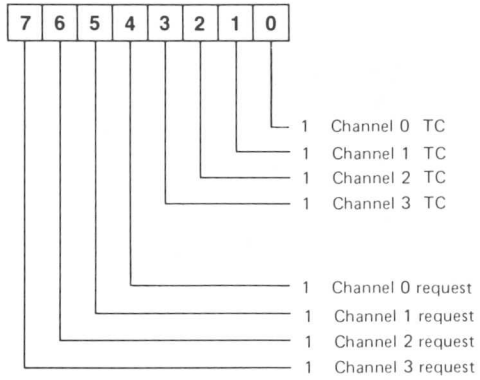
Am9511 Am9517 Am9519

REFERENCE GUIDE

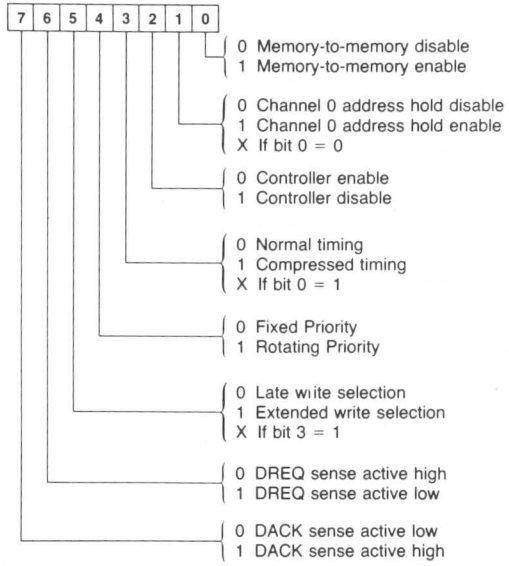


ADVANCED MICRO DEVICES

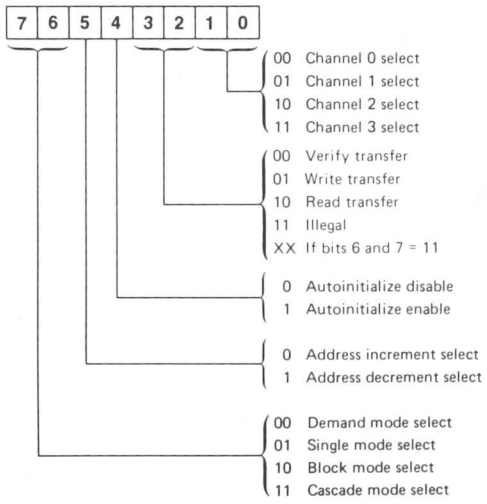
STATUS REGISTER



COMMAND REGISTER

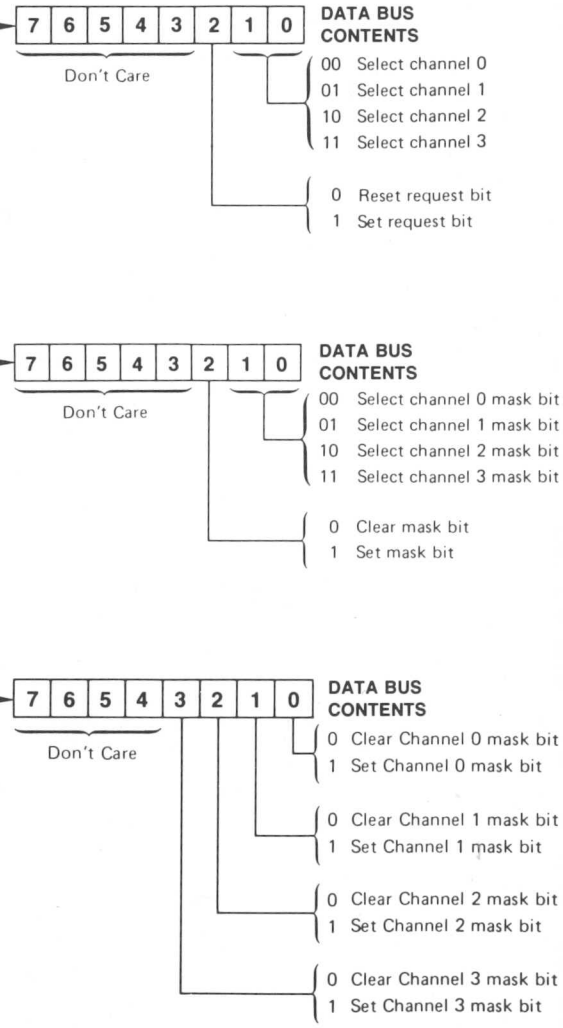


MODE REGISTER



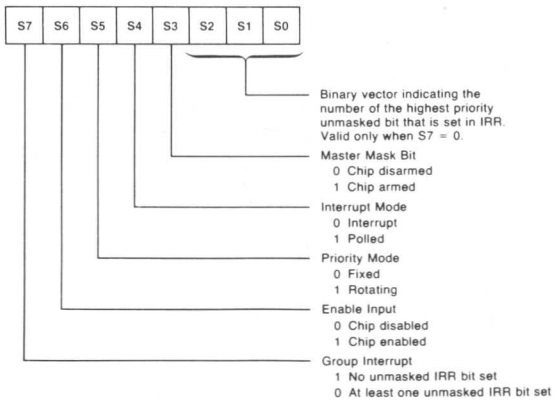
REGISTER ADDRESSING

A3	A2	A1	A0	Operation	Register
0	0	0	0	R/W	Channel 0 Address
0	0	0	1	R/W	Channel 0 Word Count
0	0	1	0	R/W	Channel 1 Address
0	0	1	1	R/W	Channel 1 Word Count
0	1	0	0	R/W	Channel 2 Address
0	1	0	1	R/W	Channel 2 Word Count
0	1	1	0	R/W	Channel 3 Address
0	1	1	1	R/W	Channel 3 Word Count
1	0	0	0	Read	Status Register
1	0	0	0	Write	Command Register
1	0	0	1	Write	Request Register
1	0	1	0	Write	Mask Register Single Bit
1	0	1	1	Write	Mode Register
1	1	0	0	Write	First/Last Bit Cleared
1	1	0	1	Read	Temporary Register
1	1	0	1	Write	Master Reset
1	1	1	1	Write	Mask Register Four Bits

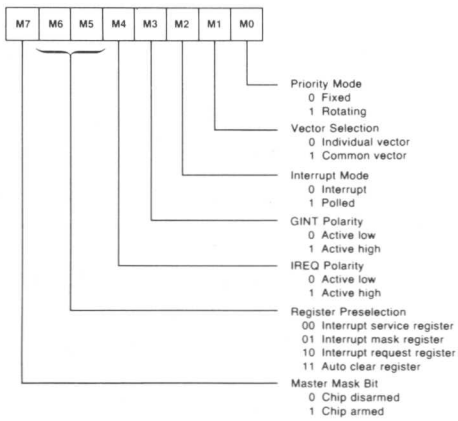


COMMAND CODE								COMMAND DESCRIPTION
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0	0	1	0	X	X	X	Clear all IRR and all IMR bits
0	0	0	1	1	B2	B1	B0	Clear IRR and IMR bit specified by B2, B1, B0
0	0	1	0	0	X	X	X	Clear all IMR bits
0	0	1	0	1	B2	B1	B0	Clear IMR bit specified by B2, B1, B0
0	0	1	1	0	X	X	X	Set all IMR bits
0	0	1	1	1	B2	B1	B0	Set IMR bit specified by B2, B1, B0
0	1	0	0	0	X	X	X	Clear all IRR bits
0	1	0	0	1	B2	B1	B0	Clear IRR bit specified by B2, B1, B0
0	1	0	1	0	X	X	X	Set all IRR bits
0	1	0	1	1	B2	B1	B0	Set IRR bit specified by B2, B1, B0
0	1	1	0	X	X	X	X	Clear highest priority ISR bit
0	1	1	1	0	X	X	X	Clear all ISR bits
0	1	1	1	1	B2	B1	B0	Clear ISR bit specified by B2, B1, B0
1	0	0	M4	M3	M2	M1	M0	Load Mode register bits 0–4 with specified pattern
1	0	1	0	M6	M5	0	0	Load Mode register bits 5, 6 with specified pattern
1	0	1	0	M6	M5	0	1	Load Mode register bits 5, 6 and set mode bit 7
1	0	1	0	M6	M5	1	0	Load Mode register bits 5, 6 and clear mode bit 7
1	0	1	1	X	X	X	X	Preselect IMR for subsequent loading from data bus
1	1	0	0	X	X	X	X	Preselect Auto Clear register for subsequent loading from data bus
1	1	1	BY1	BY0	L2	L1	L0	Load BY1, BY0 into byte count register and preselect response memory level specified by L2, L1, L0 for subsequent loading from data bus

STATUS REGISTER



MODE REGISTER



COMMAND CODE

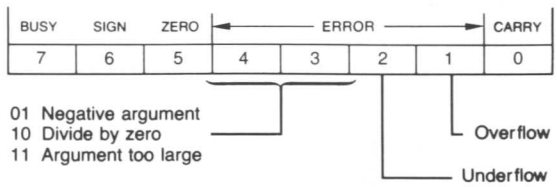
MNEMONIC	SERVICE REQUEST HEX OPCODE	NO SERVICE REQUEST HEX OPCODE	CYCLES
FIXED POINT 16-BIT			
SADD	EC	6C	17
SSUB	ED	6D	31
SMUL	EE	6E	88
SDIV	EF	6F	89
FIXED POINT 32-BIT			
DADD	AC	2C	21
DSUB	AD	2D	40
DMUL	AE	2E	194-210
DMUU	B6	36	182-218
DDIV	AF	2F	196-210
FLOATING POINT 32-BIT			
FADD	90	10	54-368
FSUB	91	11	70-370
FMUL	92	12	146-168
FDIV	93	13	154-184
SQRT	81	01	800 *
SIN	82	02	4464 *
COS	83	03	4118 *
TAN	84	04	5754 *
ASIN	85	05	7668 *
ACOS	86	06	7734 *
ATAN	87	07	6006 *
LOG	88	08	4490 *
LN	89	09	4478 *
EXP	8A	0A	4616 *
PWR	8B	0B	9292 *
DATA MANIPULATION			
NOP	80	00	4
FIXS	9F	1F	90-214
FIXD	9E	1E	90-336
FLTS	9D	1D	62-156
FLTD	9C	1C	56-342
CHSS	F4	74	23 *
CHSD	B4	34	27 *
CHSF	95	15	18 *
PTOS	F7	77	16
PTOD	B7	37	20
PTOF	97	17	20
POPS	F8	78	10
POPD	B8	38	12
POPF	98	18	12
XCHS	F9	79	18
XCHD	B9	39	26
XCHF	99	19	26
PUPI	9A	1A	16

*Weighted average execution cycle

PORT ADDRESSING

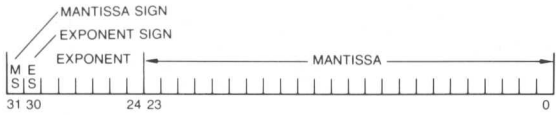
C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	Operation
0	1	0	Enter data byte into stack
0	0	1	Read data byte from stack
1	1	0	Enter command
1	0	1	Read status

STATUS REGISTER



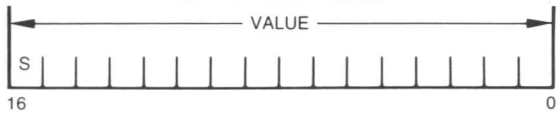
DATA FORMATS

32-BIT FLOATING POINT



SIGN-MAGNITUDE MANTISSA
UNBIASED TWO'S COMPLEMENT EXPONENT

16-BIT FIXED POINT



TWO'S COMPLEMENT

32-BIT FIXED POINT

TWO'S COMPLEMENT

Please see data sheet for additional information.